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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,004	11/13/2003	Scott D. Brandenburg	A3-1620	1003

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EXAMINER	
PHAN, THIEM D	

ART UNIT	PAPER NUMBER
3729	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,004	BRANDENBURG ET AL.	
	Examiner	Art Unit	
	Tim Phan	3729	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/03 & 3/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicants' election of Group II, Claims 11-20, filed on 12/27/05 is acknowledged.

The Restriction mailed on 12/15/05 has been carefully reviewed and is held to be proper. Applicants did not distinctly and specifically point out any logical error in the Restriction Requirement. Moreover, due to the lack of traversal on the merits, Applicants' election of Group I, claims 1-10, has been treated as an election without traverse.

Accordingly, Claims 1-10 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Group, there being no allowable generic or linking claim.

The Restriction filed on 12/15/05 is hereby **made Final**.

Applicants are required to cancel these nonelected claims (1-10) or take other appropriate action.

An Office Action on the merits of Claims 11-20 now follows.

Title

2. The following title is suggested: "Method of Developing an Electronic Module".

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 11-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukumoto et al (US 2002/0105068) in view of Brandenburg et al (US 6,180,045).

As applied to claim 11, Fukumoto et al teach several methods of manufacturing stacked semiconductor device, comprising:

- providing a developmental unit of the electronic module (Fig. 19, K15), the developmental unit comprising the motherboard (Fig. 19, 58), the multichip module (Fig. 19, items 26, 28' or 57a-c), and a circuit unit (Fig. 19, 10) connected to the multichip module, the circuit unit comprising a flexible substrate (Fig. 19, 105), instrumentation circuitry (Fig. 19 & 20, see below) mounted on the flexible substrate or board, and a

connection coupled to the flexible substrate, the flexible substrate having signal lines that electrically communicate with the multichip module, the instrumentation circuitry, and the connection, a portion of the flexible substrate or board (Fig. 19, 105) being between the multichip module (Fig. 19, 26) and the motherboard (Fig. 19, 58) and permitting electrical communication therebetween, the instrumentation circuitry not being mounted directly to the motherboard so as not to require space on the motherboard; except for specifying a connector for interfacing the connecting pad (Fig. 20, 105a).

- producing a production unit of the electronic module by eliminating or increasing the circuit unit to vary the stacked semiconductor device structure (Page 1, paragraph 2) without altering the motherboard.

Brandenburg et al teach a method of forming an overmolded electronic assembly with the pin connections (Fig. 4, 14) and the semiconductor device (Fig. 4, 16) interconnected through a thin or flexible laminate/substrate (Fig. 4, 12) for easy data signal interface to other devices.

It would be obvious to one of ordinary skill in the art at the time the invention was made to combine the two teachings by applying the pin connections or connector through a thin or flexible laminate, as taught by Brandenburg et al and not its general structure, to the methods of manufacturing stacked semiconductor device, as taught by Fukumoto et al in order to obtain an easy data signal interface with other electronic devices and it appears that the flexible wiring boards (Fukumoto et al; Fig. 19, 105) that are portionally applied to the circuit unit, the multichip module and the substrate would perform the same function as being wastefully applied to the whole system.

Fig.19

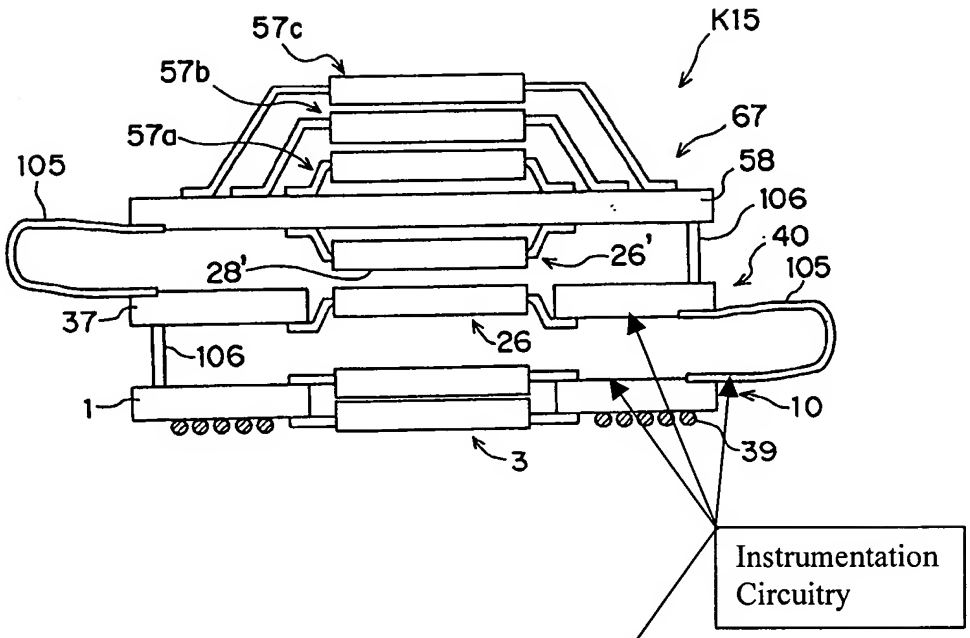
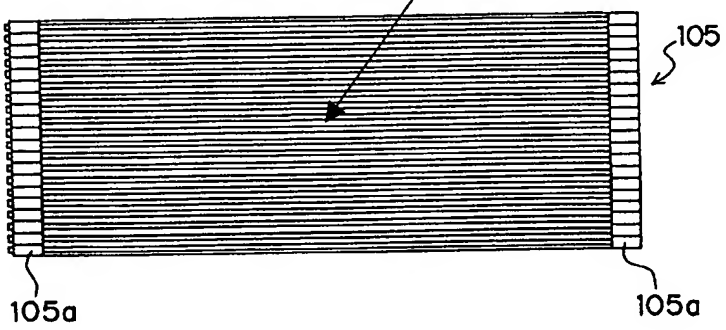


Fig.20



As applied to claim 12, Fukumoto et al in view of Brandenburg et al teach that the step of providing the developmental unit comprises placing the motherboard, the multichip module, the flexible substrate, and the instrumentation circuitry in a housing structure (Fukumoto et al;

Fig. 19, K15) that can be overmolded as taught by Brandenburg et al, and mounting the instrumentation circuitry directly to the molding or housing so as to be spaced apart from the motherboard.

As applied to claim 13, Fukumoto et al in view of Brandenburg et al teach that the step of providing the developmental unit further comprises supporting the connector (Brandenburg et al ; Fig. 4, 14) outside the molding or housing (Fig. 4, 22) with the flexible substrate in order to interface with other devices.

As applied to claim 14, Fukumoto et al teach the mounting of the instrumentation circuitry (Fig. 19, 105) directly to the multichip module (Fig. 19, 40).

As applied to claim 15, Fukumoto et al in view of Brandenburg et al teach that the step of providing the developmental unit further comprises placing the motherboard, the multichip module, the flexible substrate, and the instrumentation circuitry in a housing or molding (Brandenburg et al; Fig. 4, 22), and supporting the connector (Fig. 4, 14) outside the housing or molding with the flexible substrate or laminate.

As applied to claim 16, Fukumoto et al in view of Brandenburg et al teach that the step of providing the developmental unit further comprises individually encasing the multichip module and the instrumentation circuitry in overmolded bodies (Brandenburg et al; Fig. 4, 22).

As applied to claim 17, Fukumoto et al in view of Brandenburg et al teach that the step

of providing the developmental unit comprises placing the motherboard, the multichip module, the flexible substrate, and the instrumentation circuitry in a housing or molding (Brandenburg et al; Fig. 4, 22), and attaching a portion of the flexible substrate to the housing so that the instrumentation circuitry (Fukumoto et al; Fig. 19, 105) is spaced apart from the motherboard (Fig. 19, 58).

As applied to claim 18, Fukumoto et al in view of Brandenburg et al teach that the step of providing the developmental unit further comprises supporting the connector (Fig. 4, 14) outside the housing or molding (Fig. 4, 22) with the flexible substrate in order to interface with other devices.

As applied to claim 19, Fukumoto et al in view of Brandenburg et al teach that the step of providing the developmental unit further comprises encasing the motherboard, the multichip module, the flexible substrate, and the instrumentation circuitry in an overmolded body (Brandenburg et al; Fig. 4, 22), the instrumentation circuitry (Fukumoto et al; Fig. 19, 105) being suspended within the overmolded body so as to be spaced apart from the motherboard (Fig. 19, 58), the connector (Fig. 4, 14) projecting outside the overmolded body (Fig. 4, 22).

As applied to claim 20, Fukumoto et al in view of Brandenburg et al teach that the step of providing the developmental unit comprises mounting the instrumentation circuitry (Fig. 19, inside 105) to a printed circuit board (Fig. 19, 58) and attaching the printed circuit board to the flexible substrate (Fig. 19, 105).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Phan whose telephone number is 571-272-4568. The examiner can normally be reached on M - F, 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Vo can be reached on 571-272-4690. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have any questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A. DEXTER TUGBANG
PRIMARY EXAMINER

Tim Phan
Examiner
Art Unit 3729

tp
February 28, 2006